AN 192
Characterization Methods for Copper Technology

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Discussion

Interconnect scaling is a critical factor to increase circuit density, especially for logic and microprocessor products. The enabling technology appears to favor the use of both lower resistivity copper metal and a lower-k inter-layer dielectric (ILD). The present interconnect trend (Figure 1) shows aluminum and copper to co-exist for the 180 nm node, with copper as the dominant interconnect metal for ≤130 nm nodes.

To support this new copper technology, Charles Evans & Associates has implemented a research program to develop analytical protocols for copper, barrier, and dielectric materials of next-generation devices. We offer an extensive range of analytical tools (Table 1) and expertise to enhance your copper development program. This application note highlights some of these

Table 1. A Selection of Analytical Tools Used to Characterize Copper Processing

Analytical Tool	Information
FIB Focussed Ion Beam	Void exposure grain size defect cross section
In-Lens FE-SEM In-Lens Field Emission Scanning Electron, Microscopy	Layer thickness, step coverage, grain size defect imaging
AFM Atomic Force Microscopy	Etch depth, contact geometry, surface morphology
Dynamic SIMS Secondary Ion Mass Spectrometry	In-film metal contamination, Cu diffusion through barrier materials
SurfaceSIMS™	Surface and wafer backside contamination
TOF-SIMS Time-of-Flight SIMS	Post-CMP cleans on patterned wafers, surface metal and organic contamination
TXRF Total Reflection X-ray Fluorescence	Surface and wafer backside contamination
FE-AES Field Emission Auger Electron Spectroscopy	Killer particle identification
XPS X-ray Photoelectron Spectroscopy	Silicon oxide thickness, surface contaminant

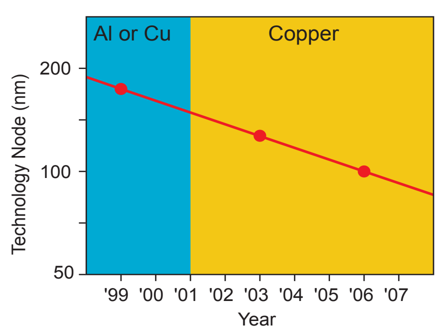

Figure 1. Probable trend of inter-connect solutions for micro-processor and logic products

Copper Processing

Copper seed deposition, copper bulk fill, and CMP processing are challenges that must be overcome to achieve acceptable yields. At this time, the yields of copper processes are typically less than 50 percent of what they are in aluminum. The most significant yield issues revolve around high aspect ratio structures and the successful filling of those structures with copper to prevent void formation.

To monitor copper processing steps, several approaches to imaging and characterizing all aspects of device geometries are available. Two of the most critical features of a successful Cu process are the barrier layer and the seed layer. In Figure 2, we see a cleave cross section through a trench region. The barrier layer (bright in this backscatter electron image) shows excellent uniformity, while the seed layer exhibits large variation in thickness going down the sidewall, and is uneven in thickness in the bottom of the trenches. The oxide deposited on top of the Cu seed is used to help ensure that the boundary of the Cu seed is retained during the cleaving process.

Figure 3 shows an SEM image of a FIB prepared cross section of Cu filled trenches that exhibit voids. The use of the FIB and the deposition of oxide avoid the problems inherent to preparing Cu cross sections using Al metallization methods.

Figure 4 is an image of the Cu seed layer in a via as seen by an Immersion-Lens FE-SEM. Sample preparation required only cleaving and conductive coating. Both the seed coverage and grain thickness can be observed.

Incorporating copper into wafer metallization processes introduces many challenges. One such challenge relates to the patterning of copper features. In a damascene process, the dielectric is patterned before the metal is deposited as a film, filling the openings in the dielectric. The film is then polished using CMP slurry to reveal the metal's features. This approach to defining copper interconnect structures achieves the desired local and global planarity while minimizing process-related defects.

TOF-SIMS has high sensitivity for detecting and imaging both atomic and molecular species. Figure 5a shows the copper ion image of a $60\ \mu m^2$ area on a patterned wafer after CMP and post-CMP clean A. The light areas are the copper lines and the dark areas the field oxide regions. Below the image is the normalized plot (Figure 5b) of the copper ion counts along the highlighted line drawn across the array in the image. Figures 5c and 5d show the comparable image and normalized plot for a wafer after post-CMP clean B. It is clear from these figures that clean B was the most effective. The copper concentration levels on the oxide areas were two orders of magnitude lower with clean B than with clean A.

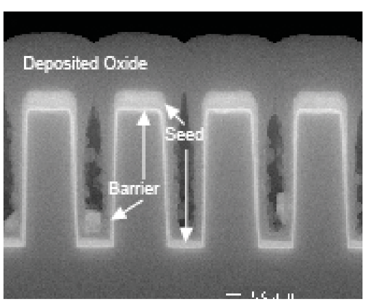

Figure 2. An oxide deposition is used to retain the dimensional integrity of the Cu seed layer for cleave cross section sample preparation. Imaging is done using the backscatter mode of an Immersion Lens FE-SEM.

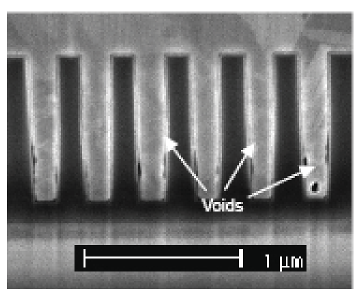

Figure 3. Secondary electron image of voids in Cu filled trenches exposed by FIB cross section.

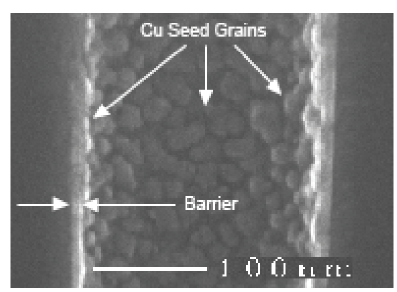

Figure 4. The Immersion Lens FE-SEM is capable of showing the Cu grain structure and coverage of a seed layer in a via.

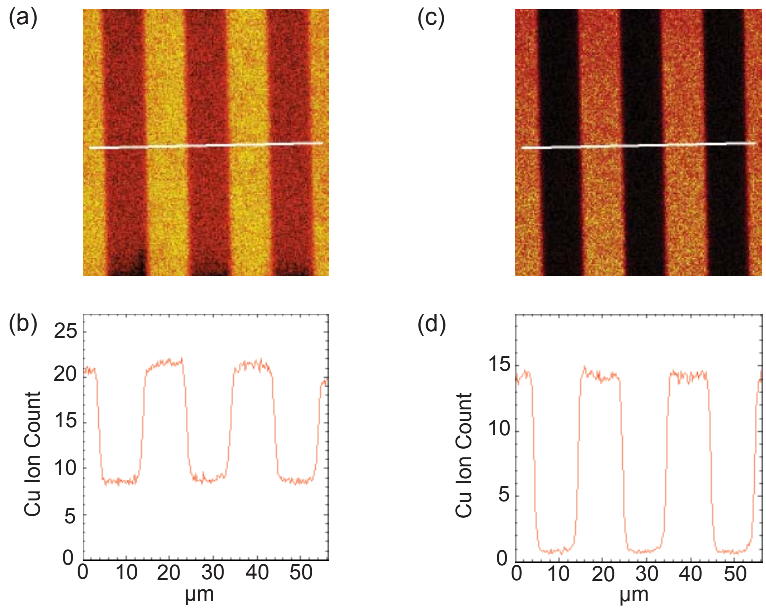

Figure 5. Copper ion images (a and c) and line scans (b and d) of a patterned wafer with copper line arrays.

Contamination

Dielectric and metal barriers to encapsulate copper are necessary to protect against copper migration from interconnect structures to neighboring dielectrics and junctions. Diffusion barriers are important since copper is very mobile at elevated temperatures. Figure 6 shows an overlay of two SIMS depth profiles. The barrier metal of sample B is not effective in preventing Cu diffusion into the low-k polymer ILD. In contrast, no copper diffusion is observed in sample A.

Effective encapsulation of copper interconnects is designed into the copper process architecture. However, copper contamination can arise from tools and equipment involved in the deposition and handling of wafers. For example, a deposition tool that coats copper films may deposit copper on the bevel of wafers. Subsequent metrology tools can be cross-contaminated from these wafers from handling the wafers. Submonolayer copper levels as high as 10^{12} atoms/cm^2 in equipment can cross-contaminate wafers. Most fabs require impurity levels to be below 10^{11} atoms/cm^2. Surface-SIMS^{TM} and TXRF can detect contaminants on silicon approaching 10^9 atoms/cm^2.

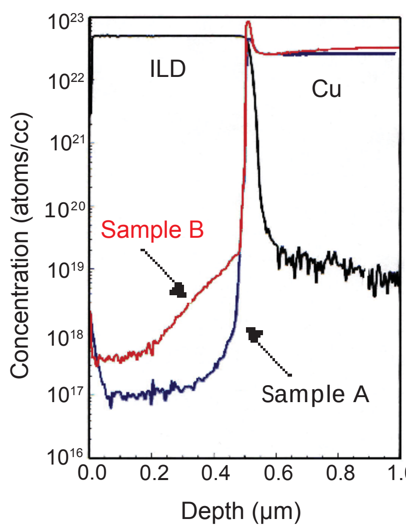

Figure 6. Overlay of two SIMS profiles showing copper diffusing into a low-k polymer in sample B.

Particles

A new process, such as copper dual damascene requires careful inspection and identification of particles to maintain a high yield. Table 2 shows a list of applicable techniques. Particles may be imaged by SEM (Figure 7), cross-sectioned using a FIB (Figure 8) and its composition determined using FE-AES (Figure 9).

A PHI SMART-200TM can perform an elemental scan and mapping on defects < 100 nm. Defect coordinate locations may be used from optical Defect Detection tools, including KLA™, Tencor™, and Inspex™.

Table 2. Analysis Techniques to Detect and Identify Small Particles

Feature size	Analysis Technique	Information Provided
≥10 nm	FE-AES	Elemental, Imaging
≥0.3 µm	FE-SEM/EDS	Elemental, Imaging
≥0.1 µm	TOF-SIMS	Elemental, Chemical
≥1 µm	µ-Raman	Chemical and molecular bonding
≥10 µm	µ-XPS	Elemental, Chemical state
≥10 µm	FTIR	Molecular groups

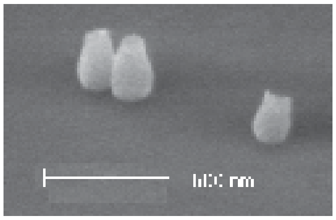

Figure 7. SEM image of defects on a surface

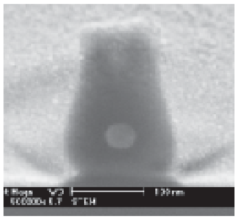

Figure 8. STEM image of a defect (shown in fig. 7) prepared using a FIB

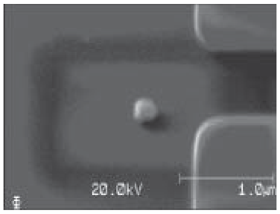

Figure 9a. AES secondary electron image

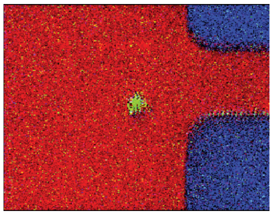

Figure 9b. AES color composite map Green = Ti, Blue = Si Nitride, Red = Elemental Si

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